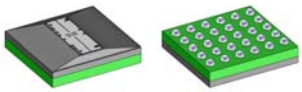
iC-LNG oBGA LNB2C

OPTO ENCODER PACKAGE SPECIFICATION

preliminary

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-LNG	oBGA LNB2C	reticle	iC-LNG oBGA LNB2C reticle



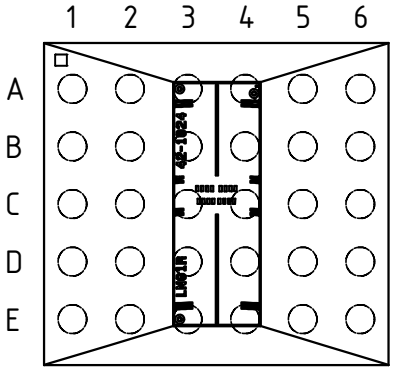
7.6 mm x 7.1 mm
RoHS compliant

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
TG1	Ta	Operating Ambient Temperature Range			-40		110	°C
TG2	Ts	Storage Temperature Range			-40		110	°C
TG3	Tpk	Reflow Soldering Peak Temperature	tpk < 20 s, convection reflow tpk < 20 s, vapour phase TOL (time on label) 8 h; please refer to customer information file No. 7 for details				245 230	°C °C

PIN CONFIGURATION

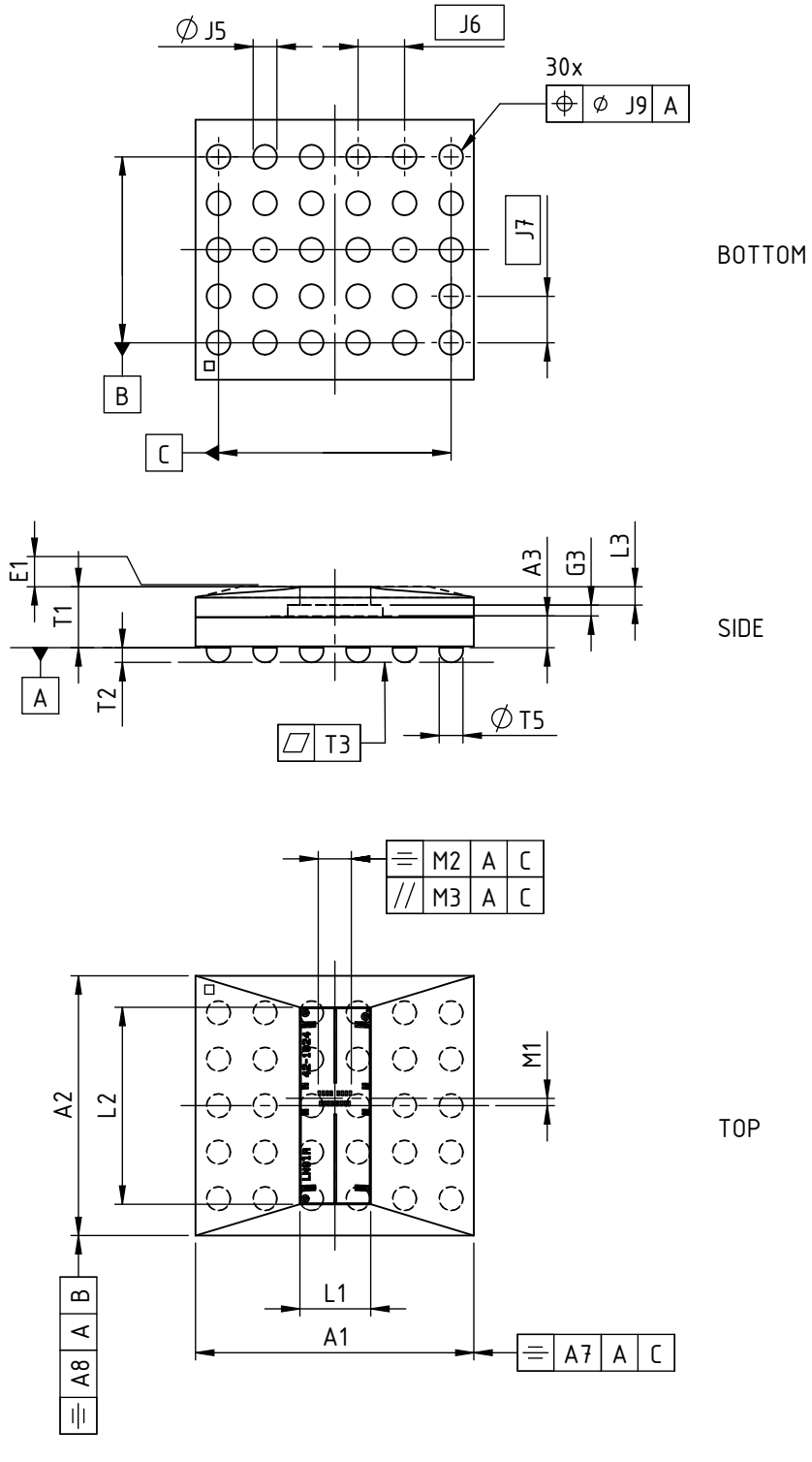
(top view)



PIN FUNCTIONS

No.	Name	Function
A1	SCK	SPI Clock Input
A2	VDD	+3 V to +5.5 V I/O Port Supply Voltage
A3	GND	I/O Port Ground
A4	LED	LED Current Control (High Side Output)
A5	VDDA	+4 V to +5.5 V Supply Voltage
A6	GNDA	Ground
B1	CS	SPI Chip Select
B2	MISO	SPI Data Output
B3	MOSI	SPI Data Input
B4	PCOS	Analog Voltage Output PCOS
B5	NSIN	Analog Voltage Output NSIN
B6	PSIN	Analog Voltage Output PSIN
C1	INCZ	Incremental Output Z / Parallel Output Bit 11
C2	TNS	Test Input NSIN / Parallel Output Bit 12
C3	TNC	Test Input NCOS / Parallel Output Bit 13
C4	TPS	Test Input PSIN / Parallel Output Bit 1
C5	TPC	Test Input PCOS / Parallel Output Bit 0
C6	NCOS	Analog Voltage Output NCOS
D1	DOUT	Shift Register Data Output / Parallel Output Bit 8
D2	DIN	Shift Register Data Input / Parallel Output Bit 9
D3	NSL	Shift Register Load / Parallel Output Bit 10
D4	INCB	Incremental Output B / Parallel Output Bit 3
D5	INCA	Incremental Output A / Parallel Output Bit 2
D6	ERR	Error Message Output
E1		N.C.
E2	PO6	Parallel Output Bit 6
E3	CLK	Shift Register Clock Input / Parallel Output Bit 7
E4		N.C.
E5	PO5	Parallel Output Bit 5
E6	POK	Power Ok Message / Parallel Output Bit 4

PHYSICAL DIMENSIONS



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DIMENSION TABLE

Item	Parameter	Conditions	Min.	Typ.	Max.	Tolerance	Unit
	Substrate						
A1	Outline X			7.60		±0.10	mm
A2	Outline Y			7.10		±0.10	mm
A3	Substrate Thickness	bottom substrate to bottom die typical value		0.90			mm
A7	Outline Symmetry X	vs. bottom metal pattern		0.20			mm
A8	Outline Symmetry Y	vs. bottom metal pattern		0.20			mm
	Chip						
G3	Chip Thickness			0.30			mm
	Bottom Metal Pattern						
J5	Lead Diameter			0.635		±0.03	mm
J6	Lead Pitch X (or Lead to Lead Distance X)			1.27			mm
J7	Lead Pitch Y (or Lead to Lead Distance Y)			1.27			mm
J9	Lead to Lead Position Tolerance				0.10		mm
	Reticle Cover						
L1	Reticle Size X			1.93			mm
L2	Reticle Size Y			5.38			mm
L3	Reticle Thickness			0.50			mm
	Encapsulation						
E1	Coating Excess	surface reticle to surface coating			0.05		mm
M1	Reticle Position vs. Bottom Metal Y	referenced to optical radius of chip center		0.20		±0.175	mm
M2	Symmetry Reticle Pattern vs. Bottom Metal				0.35		mm
M3	Parallelism of Reticle Pattern vs. Bottom Metal				0.15		mm
	Thickness Specifications						
T1	Overall Thickness	bottom substrate to top of reticle (nominal reticle thickness of 0.5 mm) [1)]	1.50	1.70	1.90		mm
T2	Solder Ball Height	drawing not to scale	0.40		0.54		mm
T3	Solder Ball Planarity				0.10		mm
T5	Solder Ball Diameter			0.635			mm

Notes:

1) Coating normally adjusted to top surface of reticle

REVISION HISTORY

Rev	Notes	Pages affected
1	Initial version	

GENERAL HANDLING INSTRUCTIONS

After opening the dry pack, devices must be mounted within 8 hours (in factory conditions of maximum 30°C / 60% RH) or must be stored at <10% RH. Devices require baking before mounting if the Humidity Indicator Card shows >10% when read at 23°C ±5°C or if the conditions mentioned above are not met. Devices may be baked for 72 hours at 100°C using high-temperature device containers (trays)

Samples
Samples may not be subject for dry pack delivery, and, in that case, are not intended for reflow soldering